IL2222 Digital design av kretsar i nanoskala för CMOS 7,5 hp

Digital Circuit Design for Nanoscale CMOS

När kurs inte längre ges har student möjlighet att examineras under ytterligare två läsår.

Fastställande

Kursplan för IL2222 gäller från och med HT08

Betygsskala

A, B, C, D, E, FX, F

Utbildningsnivå

Avancerad nivå

Huvudområden

Elektroteknik

Särskild behörighet

Högskolestudier motsvarande minst 120 hp inom teknik eller naturvetenskap, samt Engelska A.

Undervisningsspråk

Undervisningsspråk anges i kurstillfällesinformationen i kurs- och programkatalogen.

Lärandemål

After having completed the course a student should be able to:

- explain the design solution and key properties of modern nanoscale CMOS circuits

- to analyze and select design solutions of nanoscale phenomena in digital circuit and micro architecture level.

- apply theory and practice for designing modern nanoscale CMOS digital circuits and logic system towards performance, yield optimization and variability mitigation in technologies such as power reduction, clocking/synchronization, and variability mitigation.

- be familiar with the use of modern Computer Aided Design tools

- search critically literature and Internet through IEEE Explore as well as work in a team ofdesign-ers.

Kursinnehåll

In this course we study in detail all the necessary phenomena relating to logic value changes inside the logic circuit with emphasis on advanced nanoscale phenomena. The key issues in this course are to understand the nature of performance parameters such as silicon area, speed and power consumption. The structure and contents are quite similar to VLSI design courses given at many universities. The main difference is in nanoscale phenomena and bringing up power consumption issues.

This course aims to analyze and design digital integrated circuits with advanced full cus-tom and standard cell techniques based on nanoscale CMOS. We emphasize the key new phenomena and design solutions adopted to handle nanoscale phenomena at circuit and micro architecture level.

Syllabus

Review of the IC development trends. The future of IC technologies is discussed. The technology scaling models and new device level phenomena of deep submicron MOS transistors is presented.

Review of the MOS transistor physics and device model, especially the key submicron device phenomena relevant to the VLSI circuit operations

A very simplified CMOS process flow is introduced. Nanoscale CMOS issues to circuit layouts and floorplans are presented

CMOS logic from power and performance perspective are analyzed.

Power consumption in CMOS and leakage power as well as voltage scaling issues are described

Performance optimizention through micro architecture design for data paths are described

Sequential logic circuit, registers, timing and clock distribution challenge are analyzed in modern CMOS circuits

Circuit techniques for data path structures are described. Different adder and multiplier implementation schemes are introduced. Pipelining is introduced. Impact of the Vdd scaling and associated pipelining and parallelization techniques for the reduction of the data path power consumption are described.

Metal wires and interconnect as design objects are described.

Variability reduction and design optimization techniques are introduced.

Memory and Network-on-Chip architectures .

Kurslitteratur

Up-to-date issues as published in Journal of Solid-state Circuits, and in proceedings of International Conference on Solid-State Circuits (ISSCC), and European Solid-State Circuits Conference (ESSCIRC). Access through IEEE Explore required

Examination

- LAB1 - Laborationer, 3,0 hp, betygsskala: P, F
- TEN1 - Tentamen, 4,5 hp, betygsskala: A, B, C, D, E, FX, F

Examinator beslutar, baserat på rekommendation från KTH:s handläggare av stöd till studenter med funktionsnedsättning, om eventuell anpassad examination för studenter med dokumenterad, varaktig funktionsnedsättning.

Examinator får medge annan examinationsform vid omexamination av enstaka studenter.

Övriga krav för slutbetyg

Passed assignments (LAB1, 3hp)
Written exam (TEN1, 4,5hp)

Etiskt förhållningssätt

- Vid grupparbete har alla i gruppen ansvar för gruppens arbete.
- Vid examination ska varje student ärligt redovisa hjälp som erhållits och källor som använts.
- Vid muntlig examination ska varje student kunna redogöra för hela uppgiften och hela lösningen.