IL2225 Embedded Hardware Design in ASIC and FPGA 7.5 credits

Hårdvarukonstruktion i ASIC och FPGA för inbyggda system

This is a translation of the Swedish, legally binding, course syllabus.

Establishment

Course syllabus for IL2225 valid from Autumn 2012

Grading scale

A, B, C, D, E, FX, F

Education cycle

Second cycle

Main field of study

Electrical Engineering

Specific prerequisites

120 university credits (hp) in engineering or natural sciences and documented proficiency in English corresponding to English A.

Language of instruction

The language of instruction is specified in the course offering information in the course catalogue.

Intended learning outcomes

In this course students learn the logic/FSM and algorithm implementation as Embedded Hardware in a SOC Architecture realized as ASICs or FPGAs. The implementation methodology will be based on logic and high-level synthesis.This course will focus on logic and algorithm implementation as Embedded Hardware in a SOC Architecture realized as ASICs or FPGAs.

After taking this course, students are expected to know:

- Concepts of Abstraction, Domain, Synthesis and Analysis and classification of Synthesis Tools.
- Implementation styles like Full Custom, Std Cells, Mask Programmable Gate Arrays and FPGA and comparison between them.
- Coding styles for logic/FSM and Algorithms in HDL/C for efficient implementation and reuse.
- An understanding of the architectural space that the logic/FSM and high-level synthesis tools consider and infer from the HDL/C code.
- Area, Performance and Power optimisation options at logic/FSM and Algorithmic Level.
- Technology and Optimisation constraints, their implications and use in logic/FSM and High Level Synthesis.
- Libraries used in logic/FSM and High Level Synthesis.
- Links to Physical Design space and estimating the implications of physical design while doing logic/FSM and Algorithmic Design.
- Methods and concepts used to estimate/analyze the performance and power at logic/FSM and algorithmic level.
- Hardware / Software Partitioning using accelerators.
- Logic/FSM and High-Level Synthesis methodology.

Course contents

- Essential concepts for logic/FSM and Algorithm implementation using automated design flows.
- Logic/FSM Synthesis Synthesis concepts and design flow.
- HDL coding styles for efficiency, simulation, timing, clock domain crossing and power and cogestion concious.
- Technology and Optimisation Constraints and interace to foundary and back end physical synthesis flow.
- Optimizing Designs for area, performance and power in Logic/FSM synthesis.
- Static Timing Analysis.

- High Level Synthesis concepts and design flow.
- Scheduling, Allocation, Binding, Storage, Interconnect and Controller Synthesis.
- Hardware accelerators.
- Design Space Exploration.

Course literature

Principles of VLSI RTL Design by Sanjay Churiwala and Sapan Garg, Published by Springer + Lecture notes.

Examination

- TEN1 - Examination, 4.5 credits, grading scale: A, B, C, D, E, FX, F
- LAB1 - Laboratory Work, 3.0 credits, grading scale: P, F

Based on recommendation from KTH's coordinator for disabilities, the examiner will decide how to adapt an examination for students with documented disability.

The examiner may apply another examination format when re-examining individual students.

If the course is discontinued, students may request to be examined during the following two academic years.

Other requirements for final grade

- Written examination, TEN1 (4,5 credits, A-F)
- Laboratory work, LAB1 (3,0 credits, P/F)

Ethical approach

- All members of a group are responsible for the group's work.
- In any assessment, every student shall honestly disclose any help received and sources used.
- In an oral assessment, every student shall be able to present and answer questions about the entire assignment and solution.