



IL2225 Embedded Hardware Design in ASIC and FPGA 7.5 credits

Hårdvarukonstruktion i ASIC och FPGA för inbyggda system

This is a translation of the Swedish, legally binding, course syllabus.

Establishment

The official course syllabus is valid from the autumn semester 2024 in accordance with the director of first and second cycle education decision J-2024-0636. Decision date: 2024-04-15

Grading scale

A, B, C, D, E, FX, F

Education cycle

Second cycle

Main field of study

Electrical Engineering

Specific prerequisites

Knowledge in electrical circuit analysis, 6 credits, corresponding to completed course EI1110/EI1120/IE1206.

Knowledge in digital design, 6 credits, corresponding to completed course IE1205.

Knowledge in digital design and validation using hardware description languages, including experience with HDL simulators such as ModelSim or Xcelium, 6 credits, corresponding to completed course IL2203.

Language of instruction

The language of instruction is specified in the course offering information in the course catalogue.

Intended learning outcomes

On completion of the course, the students should be able to

- explain the concepts of Abstraction, Domain, Synthesis and Analysis and classification of Synthesis Tools
- explain implementation methods such as Full Custom, Std Cells, Mask Programmable Gate Arrays and FPGA and comparison between them
- use logic/FSM coding styles and Algorithms in HCD for efficient implementation and reuse
- account for the logic/FSM architectural design space and meaning of the HDL code
- optimize Area, Performance and Power with respect to logic/FSM on algorithmic level
- account for the limitations of Technology and Optimization, their implications and use in logic/FSM
- describe the libraries used in Logic Synthesis
- calculate and analyze performance and power for logic/FSM at the algorithmic level
- explain methods for Logic Synthesis and place-and-route

Course contents

- Essential concepts for logic/FSM and Algorithm implementation using automated design flows.
- Use of HDL coding styles for efficiency, simulation, timing, clock domain crossing and power and congestion conscious.
- Constraints of Technology and Optimisation and interface to foundry and back end physical synthesis flow.
- Optimizing Designs for area, performance and power in Logic/FSM synthesis.
- Static Timing Analysis.
- High Level Synthesis concepts and design flow.
- Synthesis for Scheduling, Allocation, Binding, Storage, Interconnect and Controller Synthesis.
- Hardware accelerators.

Examination

- PROA - Project work, 4.5 credits, grading scale: A, B, C, D, E, FX, F
- TENH - Oral exam, 0 credits, grading scale: A, B, C, D, E, FX, F
- TENQ - Quiz, 3.0 credits, grading scale: P, F

Based on recommendation from KTH's coordinator for disabilities, the examiner will decide how to adapt an examination for students with documented disability.

The examiner may apply another examination format when re-examining individual students.

If the course is discontinued, students may request to be examined during the following two academic years.

TENQ and PROA can give a maximum final grade of C. TENH is a voluntary oral examination for a higher final grade.

Ethical approach

- All members of a group are responsible for the group's work.
- In any assessment, every student shall honestly disclose any help received and sources used.
- In an oral assessment, every student shall be able to present and answer questions about the entire assignment and solution.