



IL2226 Embedded System Design 7.5 credits

Konstruktion av inbyggda system

This is a translation of the Swedish, legally binding, course syllabus.

Establishment

Course syllabus for IL2226 valid from Autumn 2012

Grading scale

A, B, C, D, E, FX, F

Education cycle

Second cycle

Main field of study

Electrical Engineering

Specific prerequisites

120 university credits (hp) in engineering or natural sciences and documented proficiency in English corresponding to English A.
and
Embedded Hardware Design in ASIC and FPGA

Language of instruction

The language of instruction is specified in the course offering information in the course catalogue.

Intended learning outcomes

- All the main components in an SoC: different types of memories, computational units, interconnect, I/O blocks, arbiters, power management, etc. The components non-functional properties with respect to performance, power and area are understood.
- Analyse the non-functional properties of a system: performance, power, cost.
- Dimension the components and the complete system with respect to given requirements in terms of performance, power consumption and cost.
- Design the system level clocking architecture
- Concepts and methods of testing and test pattern generation, physical design and floorplaning, IP reuse and platform based design.

Course contents

This course focuses on system level dimensioning and trade-offs aspects of Systems-on-Chip (FPGA or ASIC) design. The students study the system properties of the main SoC components, which are computation, memory and interconnect. The student learns how the components are put together into a complete system with all the important trade-offs, that have to be considered.

1. System Level Components

a. Computation

- i. Software—Superscalar, VLIW, ASIPs, Multi-core—homogeneous, heterogeneous
- ii. Hardware—ASIC, FPGAs and the emerging CGRAs

b. Storage

- i. SRAM, DRAM, Flash and emerging memory technologies
- ii. Register Files vs. SRAMs
- iii. Centralized vs. Distributed
- iv. On chip vs. off chip. Cache

c. Interconnect

- i. Interconnect hierarchy and layers
- ii. Bus types and topologies
- iii. NOC

- d. System Level Power Management
 - i. Clock Domains
 - ii. Power Domains
 - iii. DVFS
 - iv. Hibernation and Power gating
- 2. System Level Design Trade-offs
 - a. Power, Energy, Performance and Area.
 - b. The three VLSI walls–frequency, memory and power
 - c. Productivity, Reusability
- 3. Clocking and Synchronisation Issues
- 4. VLSI Physical Design
- 5. ATPG, DFT – Scan and BIST

Course literature

Lecture notes

Examination

- TEN1 - Examination, 4.5 credits, grading scale: A, B, C, D, E, FX, F
- LAB1 - Laboratory Work, 3.0 credits, grading scale: P, F

Based on recommendation from KTH's coordinator for disabilities, the examiner will decide how to adapt an examination for students with documented disability.

The examiner may apply another examination format when re-examining individual students.

If the course is discontinued, students may request to be examined during the following two academic years.

Other requirements for final grade

- Written examination, TEN1 (4.5 hp, A-F)
- Laboratory work, LAB1 (3.0, P/F)

Ethical approach

- All members of a group are responsible for the group's work.
- In any assessment, every student shall honestly disclose any help received and sources used.
- In an oral assessment, every student shall be able to present and answer questions about the entire assignment and solution.