IS1200 Computer Hardware Engineering 7.5 credits

Datorteknik, grundkurs

This is a translation of the Swedish, legally binding, course syllabus.

If the course is discontinued, students may request to be examined during the following two academic years

Establishment

On 2019-10-15, the Head of School of EECS has decided to establish this official course syllabus to apply from the spring semester 2020 (registration number J-2019-0672).

Grading scale

A, B, C, D, E, FX, F

Education cycle

First cycle

Main field of study

Technology

Specific prerequisites

Language of instruction

The language of instruction is specified in the course offering information in the course catalogue.

Intended learning outcomes

After passing the course, the student shall be able to

- Implement low-level programs in the C programming language and in an assembly language
- Implement low-level programs with input-output, timers, and interrupts
- Analyse processor microarchitectures, with and without a pipeline,
- Analyse memory hierarchies, including cache-structures.
- Compare fundamental concepts about multiprocessor computers.
- Explain and describe technical solutions both orally and in writing.

For higher grades, the student shall also be able to construct more complex programs and/or discuss and analyze concepts within the course. The details are specified in the course memo.

Course contents

The course gives basic knowledge of how a computer functions and is built-up both from a hardware and from a software perspective The course is divided into six different modules, which for example include the following basic concepts:

1. C-programming and assembler language: pointers, functions, stack, assembly language, machine language, instruction encoding and processor registers.
2. I/O system: timers, interrupts and memory mapped I/O.
3. Digital design: truth tables, gates, boolean algebra, multiplexers, decoders, adders, combinatorial nets, sequential networks and registers.
4. Processor construction: arithmetic-logic unit, data path, control unit and pipeline.
5. Memory architectures: instruction cache, data cache and virtual memory.
6. Parallel processors and programs: Amdahl's law, different variants of parallelism as well as multicore.

Note that module 3 is recommended prior knowledge to the course and comes not to be treated on lectures or labs. However, the material for module 3 will be available on the course homepage, as it is prior knowledge to module 4.

Examination

- LAB1 - Laboratory Work, 4.5 credits, grading scale: P, F
- TEN1 - Examination, 3.0 credits, grading scale: A, B, C, D, E, FX, F

Based on recommendation from KTH’s coordinator for disabilities, the examiner will decide how to adapt an examination for students with documented disability.

The examiner may apply another examination format when re-examining individual students.

Ethical approach

- All members of a group are responsible for the group's work.
- In any assessment, every student shall honestly disclose any help received and sources used.
- In an oral assessment, every student shall be able to present and answer questions about the entire assignment and solution.